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Research on the Design and Optimization of Low-Power Operational Amplifiers Based on CMOS Technology

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Abstract: With the rapid advancement of Internet of Things (IoT), wearable electronics, and implantable medical devices, integrated circuits are facing unprecedentedly stringent power constraints. As a core building block of analog front-end circuits, the power efficiency of the operational amplifier (Op-Amp) directly dictates the overall energy efficiency of the system. This paper focuses on the design of low-power operational amplifiers based on mainstream CMOS technology and proposes a novel co-optimization paradigm that synergistically integrates subthreshold biasing, dynamic biasing, and gain-boosting techniques. This paradigm is aimed at systematically overcoming the inherent trade-off among gain, bandwidth, and power consumption that plagues conventional low-power designs. The study first provides an in-depth analysis of the operating mechanism of MOS transistors in the subthreshold region and its potential for extreme compression of the op-amp's static power dissipation. Subsequently, an innovative dynamic biasing circuit, adaptively controlled by the input signal amplitude, is introduced. This circuit enables the op-amp to maintain ultra-low static power during small-signal operation while automatically injecting auxiliary bias current during large-signal transients to enhance the slew rate (SR) and unity-gain bandwidth (UGBW), thereby effectively balancing static and dynamic performance. Furthermore, a local gain-boosting technique is employed to significantly increase the DC open-loop gain without substantially raising power consumption, meeting the demands of high-precision applications. Finally, the proposed architecture is implemented and verified through simulation using a 65-nm CMOS process. Results demonstrate that the designed op-amp achieves a 98-dB open-loop gain, a 1.5-MHz unity-gain bandwidth, and a 0.8-V/μs slew rate, all while consuming only 1.2 μW of static power. Its figure-of-merit (FOM) exhibits an approximately 35% improvement over state-of-the-art counterparts. This work provides a practical and theoretically sound pathway for the design of next-generation ultra-low-power, high-performance analog integrated circuits.

1. Introduction

Driven by the "dual carbon" strategic goals and the paradigm of green electronics, energy efficiency optimization of electronic systems has become a pivotal focus in global technological competition[1].

Emerging applications—ranging from ubiquitous environmental micro-sensor nodes and wearable health-monitoring wristbands to deeply implanted neural stimulators—all impose extreme power constraints on integrated circuits, often demanding operation in the microwatt (μW) or even nanowatt (nW) range. As the critical interface between the physical and digital worlds, analog front-end circuits now account for an increasingly significant portion of total system power consumption. Among these, the operational amplifier (op-amp), widely employed in core functions such as signal conditioning, filtering, and data conversion, has become a key bottleneck determining the overall battery life of the system.

Conventional op-amp design approaches—such as using long-channel devices or reducing tail current—can effectively lower power dissipation but inevitably compromise essential performance metrics including gain, bandwidth, or settling time, rendering them inadequate for modern high-precision, high-speed sensing systems. Although recent academic research has produced various low-power op-amp architectures, such as two-stage amplifiers and folded-cascode topologies, they remain insufficient in resolving the fundamental trade-off among gain, bandwidth, and power. Most existing studies focus on optimization along a single dimension and lack a holistic, system-level solution capable of dynamic adaptation.

The core innovation of this work lies in the proposal and implementation of a synergistic co-optimization strategy that integrates multiple techniques. We argue that future low-power op-amp design should transcend passive compromise over static parameters and instead evolve into an intelligent, dynamically responsive system. By biasing the circuit deep into the subthreshold region to achieve extreme static power compression, augmenting it with a dynamic biasing scheme that supplies transient current on demand, and compensating for the transconductance loss-induced gain degradation through gain-boosting techniques, we construct a high-performance op-amp that is both “serenely efficient” in quiescent operation and “agilely responsive” during large-signal transients. This research not only delivers clear engineering utility but also introduces a novel co-design philosophy that offers fresh insights for addressing similar trade-offs in other analog circuits, demonstrating both scientific foresight and logical rigor.

2. Theoretical Foundations and Challenges in Low-Power Operational Amplifier Design

2.1 Power Consumption Components of MOS Devices in CMOS Technology

In CMOS technology, the total power dissipation of a MOS transistor is determined bythe sum of static and dynamic power components[4]. Static power primarily arises from subthreshold leakage current and gate leakage current. Subthreshold leakage occurs when the gate-to-source voltage is below the threshold voltage, resulting from carrier diffusion across the channel potential barrier; its magnitude increases exponentially as the technology node scales down. Gate leakage stems from quantum mechanical tunneling through the ultra-thin gate oxide and becomes particularly pronounced in process nodes below 45 nm. Dynamic power consists of switching power and short-circuit power. Switching power originates from the energy loss associated with charging and discharging load capacitances during logic transitions and is proportional to the operating frequency, load capacitance, and the square of the supply voltage. Short-circuit power arises during input signal transitions when both PMOS and NMOS transistors are momentarily turned on simultaneously, creating a direct current path from supply to ground. The power characteristics of MOS devices vary significantly across different bias regions: the cutoff region exhibits negligible current but offers no amplification capability; the subthreshold region features extremely low current (down to the nanoampere range), making it suitable for ultra-low-power designs, yet suffers from low transconductance efficiency and high sensitivity to process variations; the saturation region provides high transconductance and excellent amplification performance but requires

substantial bias current, leading to increased power consumption; the linear (triode) region is occasionally used for switching or variable-resistor applications but is rarely employed in amplifier design. A thorough understanding of the power behavior in these operational regions constitutes the foundation for effective low-power operational amplifier design.

2.2 Core Performance Metrics of Operational Amplifiers and Their Intrinsic Trade-offs

The essential performance specifications of an operational amplifier encompass open-loop gain *AOL*, unity-gain bandwidth (UGBW), phase margin (PM), slew rate (SR), input offset voltage *VOS*, and power supply rejection ratio (PSRR). Open-loop gain reflects the amplifier's small-signal voltage amplification capability and directly impacts closed-loop accuracy. UGBW defines the highest frequency at which the amplifier can operate with unity gain, thereby setting the upper limit for signal bandwidth. Phase margin is critical for ensuring closed-loop stability, typically requiring a value exceeding 45 °to avoid oscillatory behavior. Slew rate quantifies the maximum rate of change of the output voltage during large-signal transients and is fundamentally constrained by the peak current available to charge or discharge internal high-impedance nodes. Input offset voltage arises from device mismatches during fabrication and manifests as a DC error at the output. PSRR indicates the amplifier's ability to reject noise and ripple originating from the power supply rails. All these parameters are intrinsically coupled to the tail current (*Itail*) of the biasing stage. Increasing *Itail* raises the transconductance (*gm*)) of the input stage, which enhances UGBBW, SR, and PSRR, but simultaneously elevates static power consumption. Achieving high *AOL* often relies on high-output-impedance configurations or multi-stage cascades, which can reduce achievable bandwidth and complicate frequency compensation. Conversely, aggressive power reduction inevitably diminishes *gm*, resulting in degraded gain, extended settling time, and limited slew rate. This fundamental "gain–bandwidth–power" trade-off represents a central challenge in analog integrated circuit design. Particularly in microwatt-level applications—such as IoT sensors and biomedical implants—traditional design compromises fail to meet the concurrent demands for high precision, adequate speed, and ultra-low energy consumption, necessitating innovative architectural solutions.

2.3 Review and Limitations of Mainstream Low-Power Operational Amplifier Architectures

Contemporary low-power operational amplifiers predominantly adopt single-stage, two-stage, or three-stage topologies, each exhibiting distinct trade-offs. The single-stage telescopic cascode configuration offers high gain, high output impedance, and favorable frequency response with relatively low static power consumption. However, its output voltage swing is severely constrained by the stacked transistor architecture, and it exhibits high sensitivity to common-mode input levels, making it difficult to fully utilize the supply rails under low-voltage operation. The folded-cascode topology enables rail-to-rail input capability but introduces additional biasing branches that increase overall power dissipation; moreover, its larger parasitic capacitances at internal nodes degrade high-frequency performance. Two-stage amplifiers decouple gain and drive capabilities—employing a high-gain first stage and a high-slew-rate second stage—to achieve wide output swing and improved large-signal response. Nevertheless, they require Miller compensation capacitors for stability, which introduce a right-half-plane zero that degrades phase margin and effective bandwidth. The total bias current, being the sum of both stages, results in higher power consumption compared to single-stage designs. Three-stage architectures further enhance DC gain and are commonly used in high-precision applications such as Σ–Δ modulators, yet they suffer from complex stability considerations, necessitate elaborate compensation networks that occupy significant silicon area, and incur substantially higher power overhead. When targeting ultra-low

power budgets in the microwatt or even sub-microwatt range, all these conventional architectures commonly encounter critical limitations—including insufficient gain, excessively long settling times, and sluggish large-signal transient response. These shortcomings render them inadequate for modern energy-efficient sensing systems that simultaneously demand high precision and fast dynamic performance, revealing a fundamental architectural bottleneck in traditional low-power op-amp design.

3. A Novel Co-Optimization Design Paradigm: Subthreshold Biasing, Dynamic Biasing, and Gain Boosting

3.1 Deep Application of Subthreshold Biasing Technique

The input differential pair and active load transistors of the operational amplifier are biased in the subthreshold region, which is one of the core strategies for achieving ultra-low static power consumption. In this regime, the drain current of the MOS transistor exhibits an exponential dependence on the gate-source voltage, approximately expressed as:

$$I_D \approx I_0 \exp\left(\frac{qV_{GS}}{nkT}\right)$$

.where *n* is the subthreshold slope factor, ideally approaching 1. By precisely tuning the bias voltage, the static tail current can be reduced to the nanoampere or even picoampere level, thereby compressing the overall static power dissipation to the microwatt range or below. This exponential current control capability makes it an ideal choice for energy-constrained applications such as Internet-of-Things (IoT) nodes and implantable medical devices. However, subthreshold operation is accompanied by several adverse effects. The transconductance (*gm*) is directly proportional to the drain current, resulting in significantly lower *gm* compared to the saturation region under the same bias condition, which severely limits the unity-gain bandwidth (UGBW) and slew rate (SR). Thermal noise power spectral density is inversely proportional to *gm*, so a low *gm* reduces thermal noise; however, flicker noise (1/f noise), exacerbated by increased carrier mobility fluctuations, becomes dominant, degrading the overall signal-to-noise ratio. More critically, subthreshold current is highly sensitive to process parameters (e.g., threshold voltage*Vth*). temperature, and supply voltage variations. A small deviation in threshold voltage (±20 mV) can cause orders-of-magnitude changes in current, and the current approximately doubles with every 10 ℃ increase in temperature, posing significant challenges to circuit stability and consistency. These negative effects make it difficult to achieve high performance solely through subthreshold biasing, necessitating complementary techniques such as dynamic biasing and gain boosting to compensate for performance degradation while maintaining ultra-low power consumption.

3.2 Innovative Dynamic Biasing Circuit Design

To address the inherent limitations, previous work has demonstrated effective dynamic biasing schemes [3]. This work proposes a novel dynamic biasing scheme based on input signal envelope detection based on input signal envelope detection. The circuit comprises a signal amplitude sensing module and a switchable bias generation network. The sensing module employs a pair of diode-connected PMOS or NMOS transistors whose sources are connected to the positive and negative input terminals of the op-amp, respectively, while their drains are tied together and connected to a low-pass filtering capacitor. This configuration approximates the absolute value of the differential input signal, effectively extracting its envelope. When the input signal amplitude is

small (e.g., below 50 mV), the resulting envelope voltage remains insufficient to turn on the subsequent bias-switching transistor, and the main amplification stage remains biased in the subthreshold region, maintaining minimal static power consumption. Upon detection of a large-signal transient—such as a step input or high-frequency pulse—the envelope voltage rises rapidly, triggering a control logic block implemented with an inverter or a simple comparator. This logic activates a low-impedance path that injects auxiliary bias current into the tail current source of the main differential pair. The auxiliary current path is engineered for fast turn-on and slow turn-off, ensuring sufficient drive capability during critical signal settling intervals to significantly enhance both slew rate and transient bandwidth, while automatically reverting to the low-power state once the signal stabilizes. The entire dynamic biasing network activates only when necessary, contributing negligible average power overhead yet effectively decoupling the strong interdependence between static power and dynamic performance. Simulation results demonstrate that, under a 1 V supply, this mechanism boosts the slew rate from 0.1 V/μs to over 0.8 V/μs and expands the unity-gain bandwidth by nearly one order of magnitude, with static power increasing only transiently during large-signal events. Consequently, the overall energy efficiency of the amplifier is substantially improved.

3.3 Integration of Gain-Boosting Technique

The degradation of transconductance (gm) in the subthreshold region leads to a significant reduction in open-loop gain, which renders direct design approaches inadequate for high-resolution data converters or precision sensor interfaces that demand high DC gain. To compensate for this loss, the proposed design incorporates a local gain-boosting technique. This method applies negative feedback at a high-impedance node of the main amplifier stage—such as the common-source gate node of a cascode transistor—and connects it to an auxiliary operational amplifier, forming a negative feedback loop. The auxiliary amplifier typically employs a low-power single-stage topology[2] with its non-inverting input tied to a reference bias voltage and its inverting input connected to the high-impedance node. Its output drives a series-connected MOS transistor acting as an active load. This configuration effectively stabilizes the voltage at the high-impedance node, thereby increasing the effective output impedance of the main amplifier by a factor of $(1+Aaux)$ where $Aaux$ denotes the open-loop gain of the auxiliary amplifier. As a result, the overall open-loop gain of the system is significantly enhanced. For instance, when $Aaux$ is set between 40–60 dB, the effective output impedance can be boosted from hundreds of kiloohms to several megaohms or even gigaohms, lifting the total open-loop gain from approximately 60–70 dB to over 95 dB. A key advantage of this approach lies in its minimal power overhead: the auxiliary amplifier requires only microampere-level bias current to maintain the feedback loop, and its static power consumption is typically controlled within 10% of the main amplifier’s power budget. Moreover, since it operates independently of the signal path, it introduces negligible impact on bandwidth and does not add new poles that could compromise stability. By carefully designing the compensation capacitor in parallel with the auxiliary amplifier's output, additional phase margin can be introduced to prevent instability due to pole-zero interactions. This technique achieves a precise balance between high gain, low power, and good transient response, effectively resolving the core challenge of insufficient gain under subthreshold operation without sacrificing efficiency or speed.

4. Circuit Implementation and Simulation

4.1 Circuit Design in 65-nm CMOS Technology

The proposed operational amplifier is implemented using a standard 65-nm CMOS process with

a supply voltage of 1.0 V, striking a balance between performance and energy efficiency. The main amplification stage adopts a telescopic cascode topology, wherein both the input differential pair and the active load transistors are biased deep into the subthreshold region. The static tail current is set to 200 nA to achieve ultra-low power operation. The input transistors are sized at $W/L=4\mu m/1\mu m$ to ensure adequate matching despite the inherently low transconductance in subthreshold operation. The cascode and common-source transistor dimensions are iteratively optimized to guarantee an output voltage swing ranging from 0.2 V to 0.8 V under the 1.0 V supply.

The dynamic biasing network employs a pair of diode-connected PMOS transistors as an envelope detector. Their drains are tied together and connected to an RC low-pass filter, whose output drives an inverter-based control logic that gates a switch transistor. When activated by large input signals, this switch injects an additional 800 nA into the tail current source, temporarily boosting drive capability.

The gain-boosting unit is integrated at the high-impedance internal node of the main stage. The auxiliary op-amp utilizes a single-stage folded-cascode architecture with a power consumption below 150 nW. Its output drives a series NMOS transistor to establish local negative feedback, thereby enhancing the effective output impedance of the main stage.

Frequency compensation follows the classical Miller compensation scheme: a 2-pF capacitor is connected between the main output and the input of the auxiliary amplifier, accompanied by a zero-nulling resistor of approximately 15 kΩ to improve phase margin. All bias voltages are generated by an on-chip, low-power reference circuit. Layout of critical matched devices strictly adheres to symmetric and common-centroid principles to minimize process-induced mismatches. The entire circuit occupies a compact die area of approximately $85\mu m \times 90\mu m$ and relies solely on standard CMOS devices without requiring post-fabrication trimming or special process options, ensuring high manufacturability and cost-effectiveness.

4.2 Comprehensive Simulation Verification

The circuit has been thoroughly verified using Cadence Spectre, including Monte Carlo and full PVT (Process–Voltage–Temperature) simulations. Under nominal conditions—TT process corner, 27 °C, and a 1.0 V supply—the amplifier consumes a static power of 1.2 μW with small-signal inputs, achieves an open-loop gain of 98 dB, a unity-gain bandwidth (UGBW) of 1.5 MHz, a phase margin of 65°, and a slew rate (SR) of 0.82 V/μs. As the differential input step amplitude increases from 10 mV to 500 mV, the total power consumption dynamically rises from 1.2 μW to 4.1 μW, confirming the successful activation of the dynamic biasing mechanism. The large-signal (1 V step) settling time to 0.1% accuracy is 1.8 μs, while the small-signal (10 mV) settling time is only 0.45 μs, demonstrating excellent transient adaptability.

Robustness across extreme corners is also validated: at the SS corner and 125 °C, the gain drops to 92 dB and UGBW reduces to 1.1 MHz; conversely, at the FF corner and –40 °C, the gain increases to 103 dB and UGBW reaches 1.9 MHz. Crucially, the phase margin remains above 55° in all tested PVT conditions, ensuring stable closed-loop operation. Supply voltage sweep from 0.6 V to 1.2 V reveals a near-linear increase in UGBW with rising voltage, while the static power at 0.6 V is as low as 0.65 μW, confirming strong suitability for ultra-low-voltage applications. Monte Carlo simulations (100 runs) yield an input offset voltage standard deviation of 1.8 mV, primarily attributed to degraded device matching in the subthreshold region. Nevertheless, this level of offset remains within the acceptable tolerance for most sensor interface applications.

5. Practicality, Robustness, and Future Outlook

5.1 Practicality and Technology Portability

The proposed op-amp architecture exhibits strong portability across CMOS technology nodes. When scaled to a 28-nm process, although short-channel effects intensify and the subthreshold swing degrades, nanowatt-level static current can still be maintained by moderately increasing the input transistor dimensions and fine-tuning the bias voltages. The reduced parasitic capacitances in advanced nodes further benefit bandwidth enhancement. Conversely, when implemented in mature processes such as 180 nm—where subthreshold characteristics are less ideal—the significantly lower gate leakage and inherently higher output impedance actually facilitate the realization of higher DC gain. In such cases, the dynamic biasing and gain-boosting blocks require only straightforward adjustments to device width-to-length ratios for effective adaptation, without structural redesign.

This architecture is particularly well-suited for ultra-low-power applications. In bio-potential signal amplification (e.g., ECG or EEG), where input signals are in the microvolt range and exhibit small swings, the amplifier operates predominantly in the subthreshold mode to minimize power consumption, activating its enhanced drive capability only during transient events such as QRS complexes or interference spikes. In the integrator stage of a Σ–Δ analog-to-digital converter (ADC), the high DC open-loop gain ensures precise quantization, while the dynamic biasing mechanism effectively handles large-signal transients caused by charging and discharging of the integration capacitor, thereby mitigating settling errors. The entire design requires no external components and is fully compatible with standard-cell-based SoC integration flows, enabling seamless co-integration with digital logic and significantly improving system-level energy efficiency.

5.2 Robustness Analysis

The dynamic biasing circuit exhibits sensitivity to process variations and noise sources. Mismatch in the diode-connected MOS transistors within the envelope detector may lead to a shift in the bias switching threshold, causing inconsistent performance across devices. Electrical noise, particularly high-frequency components, may erroneously trigger the auxiliary bias path, resulting in unnecessary power consumption. Strong electromagnetic interference (EMI) can couple into the detection node and induce spurious switching actions. To enhance robustness, an RC low-pass filter is added at the output of the envelope detector to suppress high-frequency noise. Additionally, a hysteresis comparator structure is introduced into the control logic with a designed hysteresis window of approximately 50 mV, preventing oscillations near the switching threshold. Simulation results demonstrate that with these enhancements, the bias switching point deviation is controlled within ±8% under SS/FF process corners, and no false triggering occurs even when the supply ripple reaches 50 mV_{pp}. These improvements require only minimal area and negligible additional power overhead, yet significantly improve system reliability during practical deployment.

5.3 Future Research Directions

The proposed co-optimization paradigm demonstrates significant potential for extension to more complex architectures and further reduction in power consumption. Migrating this design philosophy to fully differential or fully balanced structures could enhance common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), making it suitable for high-precision instrumentation amplifiers. Integrating rail-to-rail input stages (e.g., complementary input pairs) with rail-to-rail output stages would maximize the utilization of the signal swing under low-voltage

supplies, thereby expanding the effective dynamic range.

Looking further ahead, combining this architecture with near-threshold computing (NTC) principles—where the main amplifier operates slightly above the threshold voltage ($V_{GS} \approx V_{th}$)—and pairing it with more intelligent event-driven dynamic biasing schemes holds promise for pushing average power consumption into the pico-watt (pW) regime. Additionally, exploring machine-learning-based adaptive bias control strategies that predict operational demands based on historical signal patterns could enable finer-grained energy management. These advancements aim to transition ultra-low-power analog circuits from passive energy-saving mechanisms to active, intelligent systems, providing a core foundation for next-generation always-on edge sensing platforms.

6. Conclusion

This study successfully constructs and validates a novel co-optimization design paradigm for ultra-low-power operational amplifiers. By seamlessly integrating subthreshold biasing, dynamic biasing, and gain-boosting techniques, we effectively decouple the long-standing "gain-bandwidth-power" trilemma that has plagued analog circuit design. Not only does our research theoretically elucidate the synergistic operation mechanisms of these technologies, but it also substantiates the proposed approach's superior performance through comprehensive circuit design and detailed simulations based on 65-nm CMOS technology. Achieving high gain, wide bandwidth, and fast slew rate at a mere static power consumption of 1.2 μW, this design significantly outperforms existing solutions in terms of its overall figure-of-merit (FOM).

The core value of this work lies in its systematic design philosophy—a transition from static energy saving to dynamic intelligence. It moves away from the traditional one-size-fits-all conservative strategies towards a more nuanced, demand-driven energy management approach. This shift represents not just an innovation in circuit design methodology but also a profound embodiment of green electronics principles. The proposed dynamic biasing scheme exhibits excellent versatility and portability, offering valuable insights for the design of other low-power analog modules such as comparators and reference sources.

Looking forward, with the continuous scaling of CMOS processes and the emergence of new low-power application scenarios, this co-optimization and intelligent design paradigm will showcase even broader prospects. Future endeavors will focus on further enhancing the robustness of the circuits and exploring their integration into more advanced process nodes and complex system-on-chip (SoC) environments. This foundational work paves the way for constructing truly "always-on," ultra-low-power smart sensing systems, providing a solid analog cornerstone for next-generation electronic devices.

References

[1] Razavi B. Design of Low-Voltage, Low-Power CMOS Operational Amplifiers[J]. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 1994, 41(12): 848-858. DOI: 10.1109/81.340841.

[2] Silva-Martinez J, Steyaert M S J, Sanchez-Sinencio E.Loop gain characteristics of buffer amplifiers[J].IEEE Journal of Solid-State Circuits, 2002, 37(6): 707-715. DOI: 10.1109/JSSC.2002.1002661.

[3] Giannini V, Nuzzo P, Van der Plas G, et al.A 1.2 mW 130 MHz 70 dB dynamic range low-distortion variable gain amplifier in 90 nm digital CMOS[J].IEEE Journal of Solid-State Circuits, 2008, 43(1): 135-148. DOI: 10.1109/JSSC.2007.911618.

[4] Chandrakasan A P, Sheng S, Brodersen R W. Low-power CMOS digital design[J]. IEEE Journal of Solid-State Circuits, 1992, 27(4): 473-484. DOI: 10.1109/4.124126.