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A Stable High-Order Compensated Voltage Reference without Operational Amplifier Architecture

Zhen Zhang[1,*], Chao Geng[1], Bowen Sun[1]

[1]*Chip Design Department, Academy of Shenzhen State Micro Electronics Co., Ltd., Shenzhen, 518057, Guangdong, China*
**Corresponding author: zhangzhen2@ssmec.com*

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Abstract: A Stable High-Order Compensated Voltage Reference Without Operational Amplifier Architecture is proposed in this paper, which replaces the conventional clamp method in traditional designs. And the high-order compensation enables the low-temperature drift. Specifically, the current proportional to absolute temperature circuit generates a first-order voltage proportional to absolute temperature, which is used to compensate for the first-order characteristics of the transistor, thereby producing a second-order reference voltage. By integrating higher-order, it compensates for both the second-order and higher-order terms, achieving a low-temperature drift voltage reference. The proposed circuit is simulated based on 350 nm process, which features temperature coefficient of 7.074ppm/℃, PSRR of -78.34dB, phase margin of 81.64 °, and line regulation of 1.232mV/V across the temperature range of -55℃ to 125℃ with supply voltage of 2.97V~5.55V.

1. Introduction

Reference circuits serve as the benchmark for electronic systems, with their performance directly determining the accuracy of downstream circuits. In critical modules like isolated DC/DC converters, and sensors, these reference circuits must withstand temperature drift, supply voltage (VDD) fluctuations, and process impact to deliver stable outputs [1-5]. Any deviation in the reference can lead to data conversion errors, and sensor measurement inaccuracies. Whether in consumer electronics signal processing or high-precision control systems for automotive and industrial applications, reference circuits remain the essential foundation ensuring reliable operation of electronic devices [6-10].

Traditional voltage reference faces three major bottlenecks: First-order temperature compensation cannot counteract the higher-order nonlinearity of base-emitter voltage of a transistor (VBE), making it challenging to achieve temperature coefficient (TC) of sub-10ppm/℃ [11]. Process variations and VDD fluctuations compromise output stability [12]. Existing resistance ratio compensation techniques are either process-sensitive, space-consuming, or structurally complex, and struggle to balance multiple performance parameters [13].

To address these issues, this paper designs a stable voltage reference circuit with high-order compensation using 0.35μm Complementary Metal-Oxide-Semiconductor (CMOS) process.

2. Architecture of circuit implementation

As shown in Figure 1, this paper features a high-order compensated reference without operational amplifier architecture, replacing the conventional clamp method in traditional designs. The traditional clamp design introduces an additional tail current source. Moreover, to mitigate input mismatch in amplifier architecture, larger input transistor pairs are required, occupying significant space. The advantage of this paper lies in its ability to save space while maintaining voltage clamping functionality. Additionally, the high-order compensation enables a low temperature drift. This paper comprises the Start-up circuit, current proportional to absolute temperature (IPTAT) circuit, current inversely proportional to absolute temperature (ICTAT) circuit, complementary voltage proportional to absolute temperature (ΔVPTAT) circuit, and the output voltage of reference (VBG_GEN) circuit. The core mechanism involves IPTAT generating a first-order voltage proportional to absolute temperature (VPTAT) across resistors R3 and R4 to compensate for transistor's first-order characteristics, thereby producing a second-order reference voltage. By integrating higher-order ΔVPTAT components, it compensates for both the second-order and higher-order terms, achieving a low-temperature drift voltage reference.

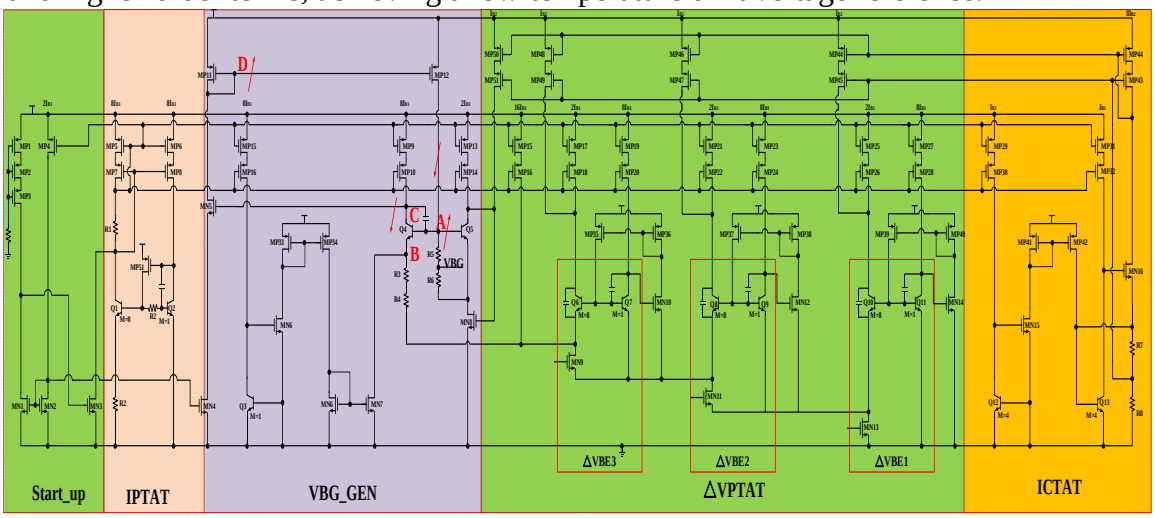

Figure 1: The architecture of the stable high-order compensated reference circuit

2.1 The Start-up circuit

The Start-up circuit, as shown in Figure 1, when powered on, MP1 ~ MP3 turn on, which increases the gate voltage of MN3, pulling down the gate voltages of PMOS transistors MP4 ~ MP8 and causing them to turn on. The gate voltage of MP4 drops, enabling MN1 and MN2 to conduct. Since MN1 and MN2 have significantly larger widths than MN3, their on-resistance is much lower than MN3's, while MN3 remains off. Simultaneously, MN4 and MN5 turn on due to the elevated gate voltage, allowing the VBG_GEN circuit to inject current and initiate operation.

The Start-up circuit enables the circuit to escape the degenerate point at the origin. Once stabilized, it automatically deactivates to reduce power consumption. Furthermore, the pull-down transistors MP1 ~ MP3 are dimensionally scaled inversely, which not only lowers the threshold voltage but also accelerates the Start-up circuit's activation.

2.2 The IPTAT and ICTAT circuit

The IPTAT circuit generates VPTAT voltage through resistors R3 and R4, while the ICTAT circuit supplies nearly zero-temperature current to the ΔVPTAT circuit by integrating IPTAT

current, thereby achieving a low-temperature drift reference. The circuit employs a folded self-biased cascode current mirror structure, which not only ensures precise current mirroring but also enhances the power supply rejection ratio. The schematic is shown as Figure 2.

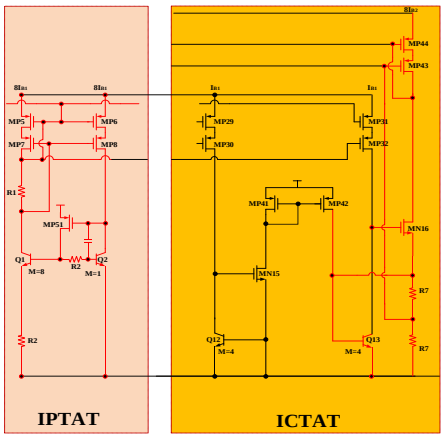

Figure 2: The architecture of the IPTAT and ICTAT circuits

To achieve high-precision current mirroring, the self-biased common-source common-gate transistors MP5, MP7, MP43, and MP44 must all operate in saturation mode. To ensure the MP5 operates in the saturation region, Eq. (1) must be satisfied.

$$|V_{GS7}| - |V_{TH5}| \le R_1 \times IPTAT \quad (1)$$

To ensure the MP7 operates in the saturation region, Eq. (2) must be satisfied.

$$R_1 \times IPTAT \le |V_{TH7}| \quad (2)$$

That is, IPTAT must meet Eq. (3).

$$|V_{GS7}| - |V_{TH5}| \le R_1 \times IPTAT \le |V_{TH7}| \quad (3)$$

Similarly, ICTAT must meet the following Eq. (4).

$$|V_{GS43}| - |V_{TH44}| \le (R_7 + r_{on16}) \times ICTAT \le |V_{TH43}| \quad (4)$$

Additionally, by inserting resistor R2 at the base of Q1 and Q2, the error caused by base current is eliminated. Since the two current mirrors in the IPTAT circuit are identical, the current generated by the IPTAT circuit can be derived through the transistor formula, as shown in Eq. (5) and Eq. (6).

$$\mathrm{V_{BE}} = \mathrm{V_T} \times \ln \frac{\mathrm{n \times I_O}}{\mathrm{M \times I_S}} \quad (5)$$

$$\Delta V_{BE_{21}} = V_{BE2} - V_{BE1} = V_T \times \ln \frac{8 \times I_{B1}}{1 \times I_S} * \frac{8 \times I_S}{8 \times I_{B1}} = V_T \ln 8 \quad (6)$$

According to the circuit, Eq. (7) can be deduced.

$$\Delta V_{BE_{21}} = V_{BE2} - V_{BE1} = V_{B2} - V_{B1} + V_{E1} = V_{B2} - \left(V_{B2} + \frac{8 \times I_{B1}}{\beta} \times R_2\right) + 8 \times I_{B1} \times (\frac{1}{\beta} + 1) \times R_2 = 8 I_{B1} \times R_2 \quad (7)$$

By combining Eq. (6) and Eq. (7), Eq. (8) can be obtained.

$$IPTAT = I_{B1} = \frac{V_T \ln 8}{8 \times R_2} \quad (8)$$

The ICTAT circuit primarily utilizes transistor Q13 to generate a negative TC current through resistor R7, as shown in Eq. (9).

$$ICTAT = 8 \times I_{B2} = \frac{V_{B13}}{2 \times R_7} \quad (9)$$

2.3 The ΔVPTAT circuit

The VPTAT circuit is designed as Figure 3: It combines three positive TC (△VBE) circuits to form a high-order compensation term for the VBG_GEN circuit, compensating for the negative temperature voltage VBE of VBG_GEN, thereby achieving a low TC.

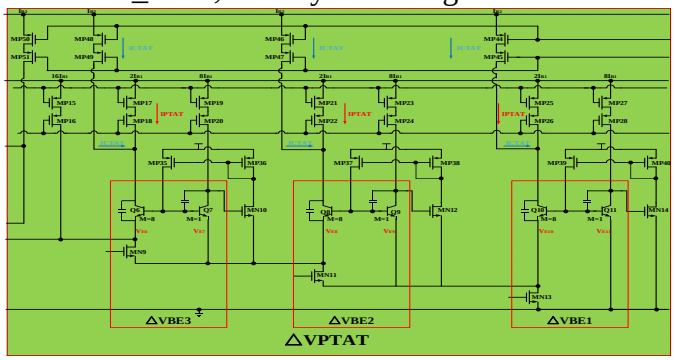

Figure 3: The architecture of the △VPTAT circuit

The voltage generated by the △VPTAT circuit, as shown in Eq. (10).

$$\Delta V_{PTAT} = V_{E6} = V_{BE7} - V_{BE6} + V_{E7} = \Delta V_{BE3} + V_{E8} = \Delta V_{BE3} + V_{BE9} - V_{BE8} + V_{E9} = \Delta V_{BE3} + \Delta V_{BE2} + V_{E10} = \Delta V_{BE3} + \Delta V_{BE2} + V_{BE11} - V_{BE10} + V_{E111} = \Delta V_{BE3} + \Delta V_{BE2} + \Delta V_{BE1} \quad (10)$$

Through the transistor formula $V_{BE} = V_T \times \ln \frac{n \times I_O}{M \times I_S}$, Eq. (11) can be obtained.

$$\Delta V_{BE1} = V_{BE11} - V_{BE10} = V_T \times \ln \frac{8 \times I_{B1}}{1 \times I_S} - V_T \times \ln \frac{2 \times I_{B1} + I_{B2}}{8 \times I_S} = V_T \ln \frac{64 I_{B1}}{2 I_{B1} + I_{B2}} \quad (11)$$

Similarly, $\Delta V_{BE2} = \Delta V_{BE3} = V_T \ln \frac{64 I_{B1}}{2 I_{B1} + I_{B2}}$, Eq. (12) can be obtained.

$$\Delta V_{PTAT} = 3 V_T \times \ln \left[\frac{64 I_{B1}}{2 I_{B1} + I_{B2}} \right] = V_T \times \ln \left[\frac{64 I_{B1}}{2 I_{B1} + I_{B2}} \right]^3 \quad (12)$$

Specifically, $I_{B1} = IPTAT = \frac{V_T \ln 8}{8 R_2}$, and $I_{B2} = ICTAT = \frac{V_{B13}}{16 R_7}$.

2.4 The VBG_GEN circuit

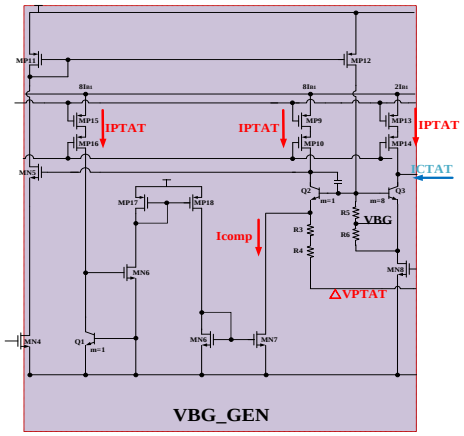

Figure 4: The architecture of the VBG_GEN circuit

The VBG_GEN circuit, as shown in Figure 4, generates the VBG, as shown in Eq. (13).

$$\mathrm{V_{BG}} = V_{B2} - \frac{V_{BE3}}{R_5+R_6} \times R_5 = V_{BE2} - \frac{R_5}{R_5+R_6} \times V_{BE3} + V_{E2} \quad (13)$$

Among, Eq. (14) can be obtained.

$$V_{E2} = [I_{E2} - I_{comp}] \times (R_3 + R_4) + \Delta \mathrm{V_{PTAT}} = \left[8 \times I_{B1} \times \left(\frac{1}{\beta} + 1\right) - \frac{8 \times I_{B1}}{\beta}\right] \times (R_3 + R_4) + \Delta \mathrm{V_{PTAT}} = 8I_{B1} \times (R_3 + R_4) + V_T \times \ln\left[\frac{64I_{B1}}{2I_{B1}+I_{B2}}\right]^3 \quad (14)$$

By combining (13) and (14), Eq. (15) can be obtained.

$$\mathrm{V_{BG}} = V_{BE2} - \frac{R_5}{R_5+R_6} V_{BE3} + 8I_{B1} \times (R_3 + R_4) + V_T \ln\left[\frac{64I_{B1}}{2I_{B1}+I_{B2}}\right]^3 \quad (15)$$

Specifically, $\mathrm{I_{B1}} = \mathrm{IPTAT} = \frac{\mathrm{V_T} \ln 8}{8\mathrm{R_2}}$, $\mathrm{I_{B2}} = \mathrm{ICTAT} = \frac{\mathrm{V_{B13}}}{16\mathrm{R_7}}$, and $\frac{\mathrm{I_{B2}}}{\mathrm{I_{B1}}} = \frac{\mathrm{V_{B13}}}{16\mathrm{R_7}} \times \frac{8\mathrm{R_2}}{\mathrm{V_T} \ln 8} = \frac{\mathrm{R_2 V_{B13}}}{2\mathrm{R_7 V_T} \ln 8}$.

The second term compensates for the first-order linear term of temperature in the expanded form of VBE, while the third term provides compensation for higher-order temperature terms.

By differentiating the VBG, the proportional relationships of resistors R2, R3, R4, R5, R6, and R7 can be determined. Adjusting these six resistors enables the creation of a reference VBG with a low TC.

3. Simulation verification results-PVT (Process, Voltage and Temperature)

After analyzing voltage reference's working principles and circuit architecture above, this paper validate its key stable parameters through simulations. These include TC, power supply rejection ratio (PSRR), loop stability (STB) and line regulation (LNR). These parameters are not independent—they often trade off performance: improving one may compromise another. Therefore, these factors must carefully be balanced during the design.

Among them, the simulation configuration under the conditions of temperature, voltage and process corner bias, with a total of 210 combinations.

3.1 TC simulation analysis

This section examines the temperature-dependent behavior of VBG across five process corners and six voltages (2.97V,3.3V,3.6V,4.5V,5V,5.55V) levels, as illustrated in Figure 5.

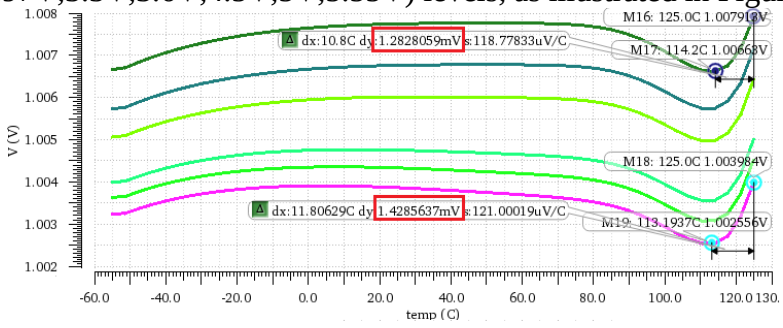

Figure 5: The TC simulation waveform

Based on the simulated TC curve, the TC of TT_corner can be calculated through the Eq. (16) and the Eq. (17), which ranges from 7.074 ppm/°C to 7.892 ppm/°C.

$$\mathrm{TC}_{max} = \frac{V_{max}-V_{min}}{\Delta T \times V_{mean}} = \frac{1.429mV}{1.006V \times 180℃} \approx 7.892ppm/℃ \quad (16)$$

$$\mathrm{TC}_{min} = \frac{V_{max}-V_{min}}{\Delta T \times V_{mean}} = \frac{1.283mV}{1.007V \times 180℃} \approx 7.074ppm/℃ \quad (17)$$

3.2 PSRR simulation analysis

The PSRR measures the circuit's immunity to VDD's noise. It is defined as the output gain caused by variations in the VDD, as shown in Eq. (18).

$$\mathrm{PSRR} = \mathrm{dB20}\left(\frac{\Delta \mathrm{VOUT}}{\Delta \mathrm{VDD}}\right) \quad (18)$$

The PSRR simulation curves for the 1Hz to 1GHz frequency are shown in Figure 6.

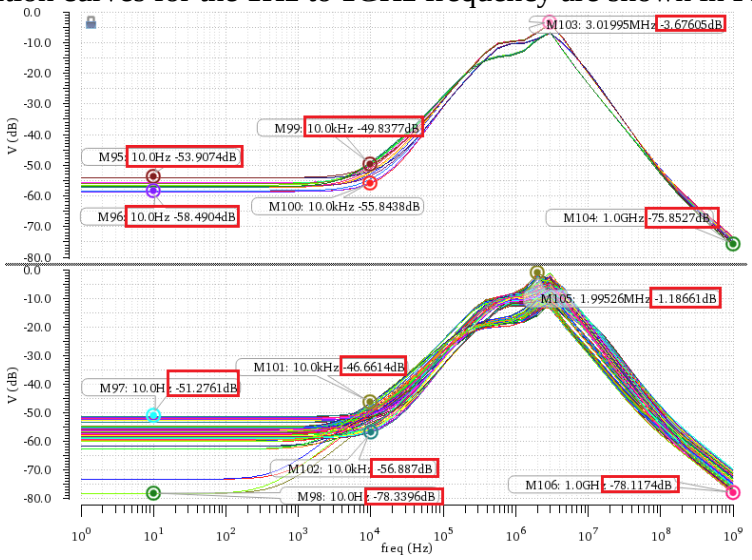

Figure 6: The PSRR simulation waveform

According to PVT conditions, the PSRR at low frequencies ranges from-51.28dB~-78.34dB, with the full-band PSRR minimum at-1.19dB. Additionally, the PSRR at high frequencies increases due to the capacitor connected at the reference output.

3.3 STB simulation analysis

The voltage reference contains a feedback loop, so its STB must be ensured to avoid oscillation. The simulation of STB under full PVT conditions is shown in Figure 7. The simulation results show that the low-frequency gain is 42.46dB~78.4dB and the phase margin is 45.41 °~81.64 °.

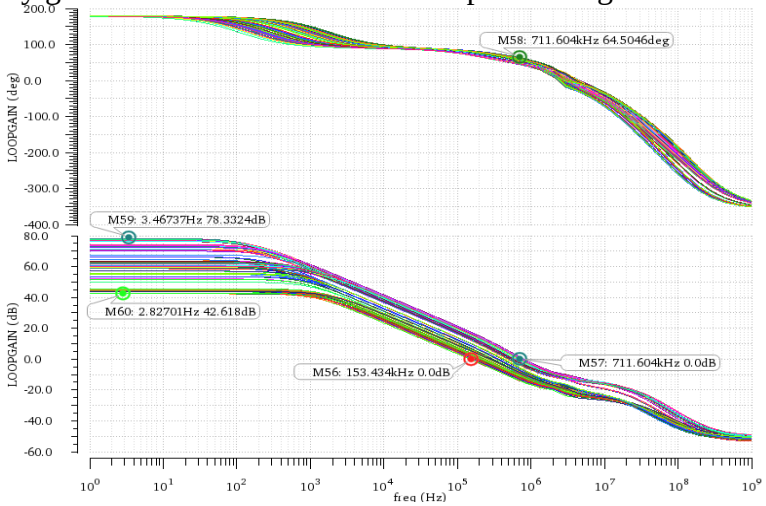

Figure 7: The STB simulation waveform

3.4 LNR simulation

Under PVT conditions, the simulation results demonstrate how voltage reference varies with VDD, which is shown as Figure 8.

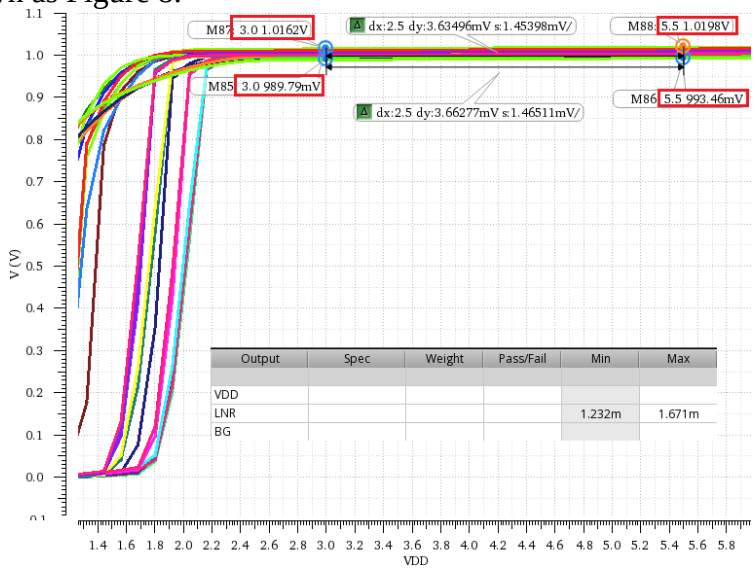

Figure 8: The LNR simulation waveform

Using the LNR calculation formula: $\mathrm{LNR} = \frac{\Delta \mathrm{VBG}}{\Delta \mathrm{VDD}}$, and calculate the simulation data. It is evident that within the 3V~5.5V voltage range, the ΔVBG varies between 1.232mV/V and 1.671mV/V.

3.5 MC (Monte Carlo) simulation analysis

To evaluate the impact of mismatch, we conducted Monte Carlo simulations to verify its performance, performing 1200 samples of voltage reference simulation as shown in Figure 9. The simulation result show that the mean reference output voltage is 1.005V, and the sample distribution is standard normal.

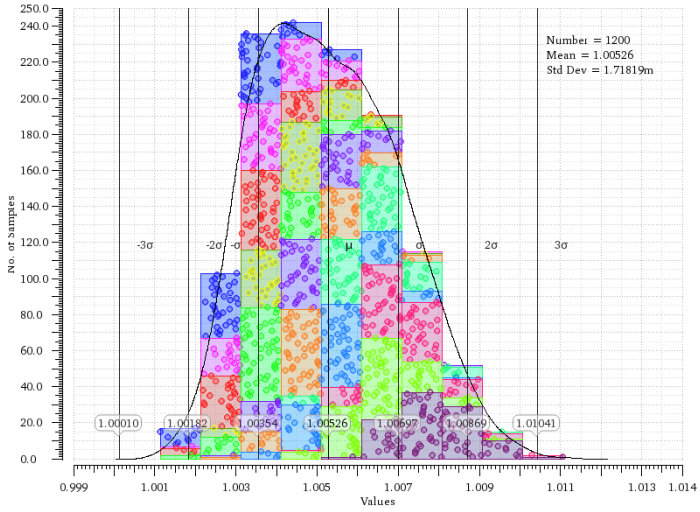

Figure 9: The MC Simulation waveform of reference voltage

Based on the simulation analysis from chapters 3.1 to 3.4, The core parameters of the proposed circuit are detailed in Table 1.

Table 1: Comparison between the proposed circuit and other circuits

	This work	[11]	[12]	[13]
Process(nm)	350	180	180	500
VDD(V)	2.97~5.55	3.3	3.3	3.3
Temperature range(℃)	-55℃~125℃	-40℃~150℃	-40℃~125℃	-5℃~125℃
TC (ppm/℃)	7.704~7.892	11.8	7.86	9.72
V_{BG}(V)	1.003~1.008	1.200	1.2181	1.196
PSRR(dB)	-78.34@(10Hz) -56.887@(10kHz)	-80(@1kHz)	-65(@1kHz)	-71(@1kHz)
LNR(mV/V)	1.232(0.1232%)	0.005%	0.048%	0.019%
Phase margin (°)	45.41~81.64	NO	NO	NO

4. Conclusions

This paper features a stable high-order compensated voltage reference without operational amplifier architecture, replacing the conventional clamp method in traditional designs, which is specifically designed for the high-performance isolated DC/DC converter as the internal voltage reference or current source for biasing, comparators and amplifiers. Utilizing 350nm CMOS process, the proposed circuit features a low TC of 7.074ppm/℃, a high PSRR of -78.34dB, a high phase margin of 81.64 °, and a low LNR of 1.232mV/V across the temperature range of -55℃ to 125℃ with VDD of 2.97V~5.55V.This precision BG

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