A novel voltage reference circuit without amplifier

Zhen Zhang

Department of Electronic Engineering, Jinan University, Guangzhou 510632, P. R. China
zhangz@stu2017.jnu.edu.cn

Keywords: voltage reference; sub-threshold; negative feedback; temperature coefficient

Abstract: A novel voltage reference circuit without amplifier is proposed in this paper. In this circuit, the difference between the two NMOS transistors operating in the sub-threshold region is applied to the resistor, thereby generating current with positive temperature coefficient, which is mirrored to the output circuit to generate voltage with positive temperature coefficient. The gate-source voltage of the NMOS operating in the sub-threshold region is added to the voltage with positive temperature coefficient, and finally reference voltage is generated that does not change with temperature, voltage and process. Compared with the traditional voltage reference circuit, the circuit is simplified by using negative feedback structure instead of amplifiers. This design is simulated based on 180 nm process and Cadence simulator. When the power supply voltage (VDD) is between 1.3 V and 2.5 V and the temperature (T) is between -80 °C and 90 °C, in the most ideal case, the temperature coefficient (TC) is 8.6 ppm/°C, the power supply rejection ratio (PSRR) is -32 dB both at 100 Hz and 10 kHz. In the typical VDD of 1.8 V, the reference voltage (VREF) is 684 mV, which can be applied to on-chip digital isolators, transceivers and temperature sensors, etc.

1. Introduction

Voltage reference circuit is an important module in the integrated circuits. It is widely used in digital circuits, analog circuits and digital-analog hybrid circuits [1-2], which provides the circuit with a stable reference voltage independent of factors such as power supply voltage (VDD), temperature (T), and process. The reference circuit mainly determines the performance of integrated circuits. Generally, a complex amplifier is applied to traditional voltage reference circuits to generate current with positive temperature coefficient [3-4]. Although the stable currents with positive temperature coefficient can be generated through this way, the use of amplifiers will inevitably cause large VDD, and eventually lead to large power consumption. In addition, the use of amplifiers also increases the complexity of circuit, which does not meet the requirements of streamlined design of circuits [5].

At the same time, traditional reference circuits are usually susceptible to temperature. Therefore, many curvature compensation circuits have been proposed to compensate the temperature of traditional reference circuits [6-7]. Although the compensated circuit is improved in temperature coefficient, the circuit is also complicated, resulting in corresponding deterioration of other parameters such as linear sensitivity.

In addition, with the continuous development of semiconductor technology, some new transistors
such as thin film field effect transistors are also used to build the reference circuit [8]. Although it can also output the reference voltage, the stability will be relatively poor, and the fab companies cannot produce tape-out. So, it is impossible to judge the actual performance.

In view of the above problems, based on the currently mature 180nm standard CMOS process, a novel voltage reference circuit without amplifier is proposed.

2. Implementation of the circuit

A new voltage reference circuit without amplifier is proposed. It is composed of start-up circuit, core circuit and output circuit, as shown in figure 1. The core circuit uses negative feedback structure instead of the amplifier in the traditional reference circuit to generate current with positive temperature coefficient and enhances the match of the branch current through the cascode structure and current mirrors. Finally, the PMOS current mirror is used to mirror the positive temperature coefficient current to the output circuit, which is added to the NMOS operating in the sub-threshold region to achieve the stability of T, VDD, and process.

![Figure 1 The proposed voltage reference circuit](image)

2.1. The start-up circuit

The start-up circuit is an essential module in the design of integrated circuits. Because the circuit does not work directly at constant VDD, it goes through a power-up process from 0 V to constant value. During this power-on process, there is a state where the circuit maintains the current of 0A, and the circuit cannot work normally in this state. Therefore, the start-up circuit is applied to ensure that the circuit can work normally. The start-up circuit is composed of MP1, MN1, MN2 and R1. R1 is directly connected to the gate and ground of MP1, so that MP1 always remains on. When the power is turned on, the gate voltage of MN2 is gradually raised to exceed the threshold voltage, where MN2 is turned on, leading that the gate voltage of MP2 ~ MP5 is pulled down, so that MP2 ~ MP5 are all turned on. At this time, the current starts to enter each branch, and the circuit works normally. When the gate voltage of the MN1 rises above the threshold voltage, and then MN1 is turned on, where the gate voltage of the MN2 is pulled down to less than the threshold voltage, causing it to turn off. After that, the power-up process is complete. MP1, MN1, and MN2 all use
large-length MOS transistors to reduce the current of the start-up circuit, thereby reducing power consumption.

2.2. The core circuit

The core circuit module is composed of MP3 ~ MP4, MN4 ~ MN7 and R2. The negative feedback loop is formed by MN4 ~ MN7, MP3 and MP4 instead of amplifier in the traditional reference circuit. When the voltage of point A rises, the voltage of point B decreases after passing MN5, and the voltage of point D rises, and then the voltage of point C rises after passing MP3, and finally the voltage of point D falls again through MN7, thereby ensuring the stability of the voltage of point D. Similarly, the voltage of point E is also maintained stable by the negative feedback structure. Therefore, the drain voltages of MN6 and MN7 operating in the sub-threshold region are maintained the same. The current with positive temperature coefficient is generated through R2, which can be written as:

\[ I_1 = \frac{V_{GS(MN6)} - V_{GS(MN7)}}{R_2} \]  

(1)

where \( V_{GS(MN6)} \), \( V_{GS(MN7)} \) are gate-source voltages of MN6 and MN7, respectively, \( I_1 \) is the current with positive temperature coefficient.

The cascode structure formed by MN4 and MN5 together with the current mirror formed by MP3 and MP4 are used to make the currents of the two branches match. The drain-source current \( I_{DS} \) of the MOS transistor working in the sub-threshold region can be expressed as [9]:

\[ I_{DS} = \mu C_OX (\eta - 1) V_F^W L e^{\frac{V_{GS} - V_{TH}}{\eta V_T}} \left[ 1 - e^{\left(\frac{-V_{DS}}{V_T}\right)} \right] \]  

(2)

where \( \mu \) is the mobility of carrier, \( C_OX \) is gate-oxide capacitance of MOSFETs, \( \eta \) is the sub-threshold slope factor of MOSFETs, \( V_T \) is thermal voltage, which can be expressed as \( V_T=KT/q \), \( K \) is Boltzmann constant and \( T \) is the absolute temperature, \( q \) is elementary charge, \( V_{GS} \) is gate-source voltage of MOSFETs, \( V_{TH} \) is threshold voltage of MOSFETs, which can be expressed as \( V_{TH}=V_{TH(T0)}-k_0T \), \( k_0 \) is the temperature coefficient of threshold voltage, \( V_{DS} \) is drain-source voltage of MOSFETs. When \( V_{DS} \geq 0.1V \), can be neglected, and Eq. (2) can be re-expressed as:

\[ V_{GS} = \eta V_T \ln \left( \frac{I_{DS}}{\mu C_OX (\eta - 1) V_F^W L} + V_{TH(T0)} \right) - K_0T \]  

(3)

The \( V_{GS} \) in Eq. (1) can be replaced by the \( V_{GS} \) in Eq. (3) and \( I_1 \) can be re-expressed as:

\[ I_1 = \frac{\eta V_T \ln N}{R_2} \]  

(4)

where \( N = \frac{I_{DS(MN6)}}{\left(\frac{W}{L}\right)_{MN6}}, \frac{\left(\frac{W}{L}\right)_{MN7}}{I_{DS(MN7)}}, I_{DS(MN6)}, I_{DS(MN7)} \) are drain-source voltages of MN6 and MN7, respectively.

2.3. The output circuit

The output circuit is composed of MP5, R3 and MN8. The current with positive temperature coefficient generated by the core circuit is mirrored by the MP5 to the output circuit, and the voltage with positive temperature coefficient \( V_P \) is generated on R3, which can be expressed as:
\[ V_p = K_1 \frac{\eta V_T \ln N}{R_2} R_3 \]  

(5)

where \( K_1 = \left( \frac{W}{L} \right)_{MP5} \). The voltage with negative temperature coefficient \( (V_N) \) in the output circuit is provided by the MN8 operating in the sub-threshold region. The temperature-independent voltage reference \( (V_{REF}) \) can be obtained by adding the positive temperature coefficient voltage and the negative temperature coefficient voltage, which can be expressed as:

\[ V_{REF} = K_1 \frac{\eta V_T \ln N}{R_2} R_3 + \eta V_T \ln \frac{K_1 \frac{\eta V_T \ln N}{R_2}}{\mu COX(\eta-1)V_F^2(\frac{W}{L})_{MN8}} + V_{TH(T0)} - K_0 T \]  

(6)

3. Simulation results

The simulation of the circuit uses 180 nm process and Cadence simulator. The simulation results of the voltage reference circuit with T, VDD and process is shown in the figure below.

Fig. 2 is the variation of \( V_{REF} \) with time during the power-on process. The power-on time is set to 10 uS, and the VDD rises from 0 V to 1.8 V. The simulation results show that after 11 uS, the circuit stably outputs the reference voltage of 684 mV, which indicates that the circuit can work normally with the help of the start-up circuit.

![Figure 2 Simulation of the power-on process](image-url)
Fig. 3 and Fig. 4 show the variations of $V_{\text{REF}}$ in the temperature range of -80 °C ~ 90 °C with the standard TT process corner and five different process corners of TT, FF, SS, snfp and spfn, respectively. Among them, under the TT process, the optimal temperature coefficient is 8.6 ppm/°C.

Figure 5 is the simulation of the PSRR in three typical VDDs of 1.3 V, 1.8 V, 2.5 V. At the stable voltage of 1.8 V and frequency of 100Hz and 10kHz, PSRR is constant value of -32dB.
The core parameters of the circuit are shown in Table 1. As can be seen from Table 1, this voltage reference circuit uses a stable process of 180 nm and achieves a minimum temperature coefficient of 8.6 ppm/°C in large temperature range of 170 °C.

Table 1: Comparison between the proposed voltage reference circuit and other circuits

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[9]</th>
<th>[10]</th>
<th>[12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology(μm)</td>
<td>0.18</td>
<td>0.065</td>
<td>0.065</td>
<td>0.065</td>
</tr>
<tr>
<td>TR(°C)</td>
<td>-80~90</td>
<td>-30~140</td>
<td>-40~80</td>
<td>0~100</td>
</tr>
<tr>
<td>TC(ppm/°C)</td>
<td>8.6</td>
<td>70/57/230</td>
<td>130</td>
<td>57</td>
</tr>
<tr>
<td>VDD(V)</td>
<td>1.3~2.5</td>
<td>0.78~1.32</td>
<td>1.08~1.32</td>
<td>0.95~1.8</td>
</tr>
<tr>
<td>$V_{re}$(V)</td>
<td>0.684</td>
<td>0.706/0.69/</td>
<td>0.33</td>
<td>0.573</td>
</tr>
<tr>
<td>PSRR@100Hz(dB)</td>
<td>-32</td>
<td>-43/-30/-30/</td>
<td>NA</td>
<td>-67</td>
</tr>
</tbody>
</table>

4. Conclusion

A new voltage reference without amplifier is proposed in this paper. The negative feedback structure replaces the traditional amplifier to generate voltage with positive temperature coefficient, combined with the gate-source voltage generated by the NMOS working in the sub-threshold region, and finally the voltage reference that does not change with T, process and VDD is generated. Based on 180 nm process and Cadence simulator, TC, PSRR and reference voltage are 8.6ppm/°C, -32dB, and 684 mV, respectively. This voltage reference can be applied to products such as digital isolators, temperature sensors and wearable smart devices.

References


